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EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	PAPER NUMBER
2183	
MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,016	ZHAO ET AL.	
	Examiner	Art Unit	
	ROBERT FENNEMA	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-6 and 8-18* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-6 and 8-18* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6 and 8-18 have been considered. Claims 1. 10, and 13-18 amended as per Applicant's request.

2. Examiner notes the entry of the following papers:

- Amendment to the claims and remarks filed 7/27/2010

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/27/2010 has been entered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-6 and 8-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the

invention. In Claim 1, it is claimed that the exiting signal is sent during a pipeline period immediately before a last cycle of the command exiting the pipeline, and that as a result of that signal, a new command is inserted into the pipeline. However, Figure 5 clearly shows new command G being inserted during Stage 1 (at the same time as A is inserted), when the last cycle of the command exiting the pipeline is Stage 3 (making the one immediately before that 2). This conflicts with the drawings, and thus one of ordinary skill in the art would not know how to make and use the invention, as the specification and drawings are not consistent with each other, thus is it unclear what is actually being done. Examiner will interpret the claim as it is written, however, clarification is required in the next action.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4-6, 8-10 and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hennessy et al. (“Computer Organization and Design, herein Hennessy).

8. Regarding Claim 1, Hennessy teaches: An overlapping command submitting method of dynamic cycle pipeline, for a chip having a pipeline including a plurality of stages, comprising the following steps:

(a) reading the command from a command buffer and storing it in a command register (Page 499: reading from the instruction memory and storing in the IF/ID pipeline register);

(b) decoding the command (Page 499; Page 450 Decode stage);

(c) preprocessing operators of the command (Page 469 Fig. 6.29), preparing initial operators of each stage of the pipeline, and storing them into an initialization register (Page 499 storing in ID/EX pipeline register);

(d) judging whether the pipeline is not full, if it is not full, directly inserting a new command (489-491 absent a stall, new instruction is automatically inserted), otherwise, waiting for an exiting signal from the command in the pipeline, the exiting signal being sent during a pipeline period immediately before a last cycle of the command exiting the pipeline (Page 492, Figure 6.46, the forwarding unit's control signals to the ALU mux inputs, which are available as soon as it finishes the ALU stage, in the memory stage, which is one stage before the last cycle it is in the pipeline),

(e) after receiving the exiting signal, judging whether there is command relevance between the new command to be inserted and an old command to exit, if yes, then inserting the new command after the old command exit (Pages 476-477, if instruction B depends upon instruction A, it must be inserted after instruction A exits); otherwise, performing a next step (if there is no dependency, then there is no need to stall and wait);

(f) when the old command is in the last cycle of the pipeline, inserting the new command into the pipeline, wherein the new command is sent to a same pipeline stage

as the old command (Page 481, Figure 6.37, a command can be entered into the pipeline as soon as the command upon which it depends has it's result (in its last cycle), and is inserted in the first stage of the pipeline, which is the same stage as the old command was present in);

wherein the new command and the old command each contain a field (Page 477, an operand),

wherein step (e) includes determining whether there is any field conflict between the new command and the old command (Page 478, detecting the hazard),

wherein if there is any field conflict between the new command and the old command, then a field branch is created (Page 492, the multiplexer connected to the ALU), the field branch including a major current register for storing the field of the new command (Page 492, the major current register corresponds to the value read from the register file) and a branch current register for storing the field of the old command (Page 480, the pipeline register holding the forwarded data), the field of the new command being added into the pipeline when submitting (Page 481, see the timing chart, the value is read from the register file when it leaves the register file stage), and the field of the old command being entered into the branch current register and maintained in the field branch until the old command uses the field for the last time (Page 480),

wherein the major current register and the branch current register are connected to a hardware processing module through a multi-route switch (Page 492, the multiplexer is the switch),

wherein if the new command is processed by the hardware processing module, the hardware processing module receives an input of the major current register in which the field of the new command is stored, and if the old command is processed by the hardware processing module, the hardware processing module receives an input from the branch current register in which the field of the old command is stored (Page 492 and 481, the forwarding logic selects either the old value or the new value, depending on which is appropriate, and sends that value to the processing module (the ALU)), and

wherein if there is no field conflict, a field switch is conducted in a corresponding pipeline segment after submitting (Page 466, the value is read from the register file if there is no required forwarding).

9. Regarding Claim 4, Hennessy teaches: The command submitting method of Claim 1, wherein the exiting signal is released two stages before the new command enters the pipeline stage (Page 492, the forwarding from memory to the ALU stage a 2-stage difference).

10. Regarding Claim 5, Hennessy teaches: The command submitting method of Claim 1, wherein the command relevance means that the new command and the old command cannot share the hardware processing module in the same pipeline stage (Pages 476-477).

11. Regarding Claim 6, Hennessy teaches: The command submitting method of Claim 1, wherein in the Step (e), it is also judged in which stage of the pipeline field switch shall be conducted for the new command and the old command, and the field switch is completed in the corresponding pipeline stage where the new command and old command overlaps (Pages 476-479 and 492, the forwarding logic has to choose the appropriate feedback path).

12. Regarding Claim 8, Hennessy teaches: The command submitting method of Claim 1, characterized wherein in the Step (c), it is required to provide an initial status of each command when each command enters the pipeline (Page 469 Fig. 6.29 -- every instruction has its initial status provided).

13. Regarding Claim 9, Hennessy teaches: The command submitting method of Claim 1, wherein each command includes reading/writing memory commands (MIPs data transfer instructions), reading/writing control register commands (MIPs move instructions) and various searching commands (MIPs Arithmetic Instructions that search for operands; moreover, all instructions can be used as part of searching algorithms).

14. Regarding Claim 10, Hennessy teaches: A chip on which the method according to Claim 1, is carried out having the dynamic cycle pipeline, comprising: interface of host computer (Page 499), input buffer (IF/ID pipeline register), command processing unit (Control), and result unit (Write Back Stage); the command processing unit

comprises: command interpreter (Multiplexers receiving control signals & ALU control) and pipeline performing unit (anything in 499); characterized in that the command interpreter further comprises: command buffer controller (pipeline registers), command register (portion of IF/ID pipeline register holding opcodes), operator processing unit (ALU control), pipeline initialization register and control automaton (EX/ME pipeline register/ALU control), which are connected in order; the control automaton controls the command buffer controller to read a command from the command buffer (ALU control completes this), and stores the command into the command register; the control automaton decodes the command (Decode stage), and controls the operator processing unit to prepare initial operators of each pipeline stage according to a type of the command, and stores them into the pipeline initialization register (499),

wherein the command processing unit sends the new command to the same pipeline stage as the old command when the exiting signal of the old command is received, or there is no command relevancy between the new command and the old command, and the old command is in the last cycle of the pipeline (Page 481, Figure 6.37, a command can be entered into the pipeline as soon as the command upon which it depends has it's result (in its last cycle), and is inserted in the first stage of the pipeline, which is the same stage as the old command was present in, and if it does not depend upon the old instruction, then it can be inserted at any point).

15. Claims 15-18 are substantially similar to Claim 10, and are rejected for the same reasons set forth in the Claim 10 rejection above.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 2, 3, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy, further in view of Vaglica (U.S. Patent No. 5,084,814).

18. Regarding Claim 2, Hennessy teaches: The method of Claim 1, but fails to teach: wherein the Step (b) also includes a step of judging whether there is an illegal command, if there is, then deleting the illegal command and returning to Step (a), otherwise, conducting the next step.

Vaglica discloses an illegal instruction detector and going to the next instruction if such a detection is made (Column 9, Lines 48-68).

Hennessy is silent towards any detection of illegal commands, and deleting them. However, Vaglica discloses a breakpoint system in which there is an illegal instruction detector, which allows the system to ignore the illegal instruction, and to instead execute the next instruction (Column 9, Lines 63-68). Vaglica further discloses that this detector provides several advantages, such as better data support features without requiring significant size for a debugging unit (Column 1, Lines 50-65). Given this

advantage, one of ordinary skill in the art would have been motivated to implement a system which can detect illegal instructions, and perform a variety of steps as a result of it, including deleting and ignoring it.

19. Regarding Claim 3, Vaglica teaches: The command submitting method of Claim 2, wherein said illegal command includes: a command with an incorrect command code and/or carrying unreasonable command parameters (Column 9, Lines 48-68).

20. Regarding Claim 11, Hennessy teaches: The command submitting method of Claim 2, wherein the exiting signal is released two stages before the new command enters the pipeline (Page 492, the forwarding from memory to the ALU stage a 2-stage difference).

21. Regarding Claim 12, Hennessy teaches: The command submitting method of Claim 2, wherein the command relevance means that the new command and the old command cannot share the hardware processing module in the same pipeline stage (Pages 476-477).

22. Claims 13 and 14 are substantially similar to Claim 10 (but depending upon Claims 2 and 3 respectively), and are taught by Hennessy for the reasons disclosed in the Claim 10 rejection above.

Response to Arguments

23. Regarding the Applicant's remarks towards the 112 second paragraph rejection of Claim 4, Examiner has noted the Applicant's response, and has withdrawn the rejection in view of Applicant's clarification.

24. Regarding Applicant's remarks towards the 112 first paragraph rejection of the claims, Applicant has argued that the subject matter of Claim 1 is adequately described in the specification. However, upon reading the section of the specification regarding Claim 5, Examiner is still very confused as to what is actually going on. Figure 5 appears to show that command "G" is inserted into the pipeline at the same time that "A" is, and that they exist and execute simultaneously until a time that "A" leaves, and then "G" continues alone. This is not what is described, but what is shown in the drawing. However, Examiner notes that upon a review of this section of the specification, it does appear to have written description, so Examiner has withdrawn the written description rejection, but has introduced an enablement rejection of the claims for the same reasons. Examiner does not understand what is being shown or described by Figure 5 and the accompanying support for it, thus one of ordinary skill in the art would not be able to make or use the invention of inserting a command to the same pipeline stage as the old command upon receiving the exiting signal, when it appears that in fact the new command was always in the pipeline. If the drawing is the object at fault, Examiner strongly recommends Applicant attempt to show a clearer example of

how it works (without introducing new matter), as the current Figure 5, to the Examiner, makes things far less clear the more the Applicant explains what they are doing.

25. Regarding Applicant's arguments towards the art rejections of the claim, Examiner is not persuaded, and has maintained the rejection. Applicant has argued that Hennessy is silent towards when the old command is in the last cycle of the pipeline, inserting the new command into the pipeline, where the new command is sent to the same pipeline stage as the old command. However, Examiner notes that this can be interpreted such that it reads on all pipelines that have ever existed. When one instruction leaves the pipeline, another one enters. Applicant has not explicitly claimed that the new command enters the same pipeline stage that the old one exits from, only that it enters at "a same pipeline stage as the old command", but does not clarify which stage that happens to be, it could be any stage the old command happened to exist in. The implication appears to be that it would enter at the same stage that the old command exited at, however, neither Applicant's drawings or specification appear to show that, as noted above, Applicant's Figure 5 clearly shows command "G" entering the pipeline in the first stage, not the fourth stage (although "G" is alone in the fourth stage after "A" exits, it is not clear what is going on in stages 1-3, as the drawing seems to suggest that "G" is present in those and executing as well, even though such a thing is not described and would generally not be how a typical pipeline would operate (and would be borderline impossible, especially if "G" depended upon "A" in any way).

26. In the next response, Examiner requests that Applicant provide a detailed, written explanation of what is actually occurring (Examiner notes that an interview was conducted where Applicant explained the subject matter, however, it was long enough ago that Examiner does not have sufficient notes to remember the entirety of what was discussed, which is why a written record would be a great help, as Examiner can continue to refer to it in the future). As Examiner has noted above, it is extraordinarily unclear what is actually occurring in this system, as the specification and drawings do not appear to relate to each other, and Examiner simply does not understand the explanation in the specification, and no examples have been provided to help overcome this. If Applicant truly is removing an instruction from the middle of a pipeline, and putting a new instruction in that same stage that the old instruction exited, and continuing execution, then Examiner is not aware of any art which does that, and would potentially be allowable, however, Examiner is not sure if the specification and drawings provided enable such a limitation (the drawings do not seem to show that, and even if they did, it is not clear if there is sufficient explanation in the specification to explain how such a system actually operates, and how one would make or use it). If the invention, however, is simply that upon a command exiting the pipeline, a new command enters the pipeline in response, Examiner asserts that this is how all pipeline systems work, and Examiner is not clear what the novelty would be. In any case, Examiner requests that Applicant provide a written explanation addressing these issues, and show support for the inventive concept in the specification, so Examiner can fully understand the invention, and how it is enabled, because currently, Examiner either sees the invention

as inherent, or not described in sufficient detail to be patentable, due to the confusing specification, and requests Applicant's assistance in overcoming this problem.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT FENNEMA whose telephone number is (571)272-2748. The examiner can normally be reached on Monday-Thursday, 9:30-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Robert Fennema/
Primary Examiner
Art Unit 2183